CLAIMS

We Claim:

1. A method for reviewing voltage contrast defects on a semiconductor specimen comprising:

turning on an electron flood gun;

applying a surface charge to a semiconductor specimen by using the flood gun;

turning off the electron flood gun;

using an electron beam generator to direct an electron beam upon the surface of the specimen, wherein the electron beam causes secondary electrons to emanate from the specimen;

detecting the secondary electrons in order to locate voltage contrast defects; and

reviewing the located voltage contrast defects.

2. A method as recited in claim 1 wherein the surface charge is applied to the entire surface of the specimen.

3. A method as recited in claim 1 wherein the surface has a negative or positive charge.

4. A method as recited in claim 1 wherein the operations of claim 1 are repeated such that during each iteration, voltage contrast defects in a new sub-region are detected and reviewed.

5. A method as recited in claim 1 further comprising:

reapplying a surface charge to the semiconductor specimen using the flood gun when the charge on the specimen is determined to be insufficient for voltage contrast effects to manifest.

6. A method as recited in claim 1 further comprising:

positioning a specimen charge electrode above the semiconductor specimen; and

while the flood gun is turned on, biasing the specimen charge electrode at a certain voltage level in order to obtain a desired charge amount on the semiconductor specimen.

7. A method as recited in claim 6 wherein the specimen charge electrode is negatively biased whereby a negative charge is applied to the semiconductor specimen.

8. A method as recited in claim 6 wherein the specimen charge electrode is positively biased whereby a positive charge is applied to the semiconductor specimen.

9. A method as recited in claim 1 further comprising:

supporting the semiconductor specimen with a specimen stage, wherein the semiconductor specimen and the specimen stage are in electrical contact; and

biasing the specimen stage at a certain voltage level in order to obtain a desired surface charge amount on the semiconductor specimen.

10. A method as recited in claim 9 wherein the specimen stage is positively biased whereby a negative charge is applied to the semiconductor specimen.

11. A method as recited in claim 9 wherein the specimen stage is negatively biased whereby a positive charge is applied to the semiconductor specimen.

12. A method as recited in claim 1 wherein the operation of reviewing the located voltage contrast defect involves energy dispersive x-ray analysis techniques or cross-sectioning tools.

13. A method as recited in claim 1 wherein the electron beam generator produces an electron beam having a current level approximately within the range of 10-50 pico Amps.

14. A method as recited in claim 13 further comprising:

detecting voltage contrast defects within features on the semiconductor specimen that have high aspect ratios.

15. A method as recited in claim 1 wherein a scanning electron microscope inspection system is used for review.

16. A charged particle beam system for use in reviewing a semiconductor wafer comprising:

an electron beam generator that generates and directs an electron beam towards the semiconductor wafer;

an electron beam column through which the electron beam travels towards the semiconductor wafer;

a sample stage that secures and supports the semiconductor wafer; and

at least one charge depositing device for adding a large amount of surface charge to the semiconductor wafer.

17. A charged particle beam system as recited in claim 16 further comprising:

a stage bias regulator that is attached to the sample stage and which is used to regulate the electrical bias of the sample stage, whereby regulating the electrical bias of the sample stage can assist in adjusting and obtaining a desired surface charge of the semiconductor wafer.

18. A charged particle beam system as recited in claim 16 further comprising:

a bias regulating electrode that is positioned above the semiconductor wafer, the electrical bias of the bias regulating electrode being controlled in order to adjust and obtain a desired surface charge of the semiconductor wafer.

19. A charged particle beam system as recited in claim 16 wherein the current level of the electron beam is in the range of 10-50 pico Amps.